IN THE SPECIFICATION:

(1) The paragraph from page 1, line 21 to line 30 has been amended as follows:

In general, in a semiconductor test device, a test pattern signal is input into a semiconductor device (device under test: DUT) which is a test object, a response signal output from the DUT is compared with an expected pattern signal to judge agreement/disagreement, and accordingly the DUT is tested. Moreover, the semiconductor test device usually ~~comprises~~ includes a timing generation circuit (TG) which generates a timing of a waveform ~~to be applied to the DUT~~ in order to apply a test signal to the DUT at a predetermined timing.

(2) The paragraph from page 2, line 4 to line 9 has been amended as follows:

As shown in ~~the figure~~ FIG. 10, the memory test device ~~comprises~~ includes: a timing generation circuit (timing generator: TG) 1; a pattern generation unit 2; a waveform formatter 3; a logical comparison unit 4; and a failure analysis memory unit 5, ~~and constitutes~~ thereby constituting a memory test device for testing a memory M ~~to be tested~~.

(3) The paragraph from page 2, line 4 to line 9 has been amended as follows:

The pattern generation unit 2 generates an address signal to be applied to the memory M to be tested which is a test object, test pattern data, control signal, and ~~an~~ expected

value data to be applied to the logical comparison unit 4 in accordance with the reference clock generated by the timing generation circuit 1.

(4) The paragraph from page 2, line 29 to page 3, line 4 has been amended as follows:

On inputting the response signal from the memory M to be tested, and the expected value data generated by the pattern generation unit 2, the logical comparison unit 4 compares both the data to detect the agreement/disagreement. Accordingly, it is judged whether or not ~~a test~~ the memory ~~110~~ M under test is satisfactory.

(5) The paragraph from page 3, line 5 to page 3, line 12 has been amended as follows:

Fail data is inputted into the failure analysis memory unit 5 in a case where the response signal from the memory M to be tested disagrees with the expected value data. The fail data is stored in a memory cell corresponding to the address signal output from the pattern generation unit 2. The fail data stored in the failure analysis memory unit 5 is separately read out and used in analyzing ~~a predetermined~~ the failure of the memory M.

(6) The paragraph from page 3, line 14 to page 3, line 16 has been amended as follows:

FIG. 11 is a block diagram showing details of a conventional timing generation circuit ~~disposed~~ incorporated in the semiconductor test device described above.

(7) The paragraph from page 3, line 25 to page 4, line 1 has been amended as follows:

In this conventional timing generation circuit, the timing data stored in the timing memory 110 is set in the down counter 120, and the set timing data is loaded by the load signal of the counter load enable selection circuit 130 to thereby ~~make a~~ decrement the timing data by one in synchronization with each occurrence of a CLK signal in the down counter 120.

(8) The paragraph from page 4, line 7 to page 4, line 19 has been amended as follows:

Specifically, to operate the timing generation circuit actually in the semiconductor test device, any one of column-direction addresses (Adr: 0 to Adr: n-1 shown in FIG. 11) of ~~a TMM 10~~ the TMM 110 is designated, accordingly the data of a row-direction bit width (m bits b0 to bm-1 in an example shown in FIG. 11) stored in the address is set in the a down counter 20, and timing data can be loaded by the load signal of the counter load enable selection circuit 130 to count down. Thus, in the conventional timing generation circuit, when the timing data indicating a desired timing is stored in the TMM, for example, a timing signal can be generated which is indicated by a delay time which is an arbitrary integer ~~times~~ multiple of a CLK signal period.

(9) The paragraph from page 5, line 4 to page 5, line 15 has been amended as follows:

However, in the conventional timing generation circuit in which a delay amount (e.g., 16 μs or less with a 20-bit width, etc.) is determined by the bit width (row direction) of the TMM in this manner, in order to handle a longer delay amount, it is necessary that a memory configuration of the TMM is changed, and the row-direction bit width is added. Moreover, it has been necessary to add a bit number per phase of the next-stage down counter. Therefore, to ~~lengthen~~ increase the delay amount, a circuit scale of the timing edge generation unit enormously increases, and a problem has occurred that the cost of a gate array ~~cost increases in~~ for establishing the timing generation circuit significantly increases.

(10) The paragraph from page 5, line 20 to page 5, line 29 has been amended as follows:

The present invention has been proposed to solve the ~~problem of~~ above-noted problems involved in the conventional art, and an object is to provide a timing generation circuit which is capable of increasing a maximum delay amount ~~or~~ as well as increasing a timing set number without changing a configuration of a timing memory containing timing data and which realizes ~~a~~ several types of TGs by one type of hardware configuration and ~~in which~~ enables low-cost device measurement ~~is possible, and~~. Another object of the present invention is to provide a semiconductor test device ~~comprising~~ incorporating this timing generation circuit.

(11) The paragraph from page 6, line 2 to page 6, line 23 has been amended as follows:

To achieve the above object, according to the present invention, there is provided a timing generation circuit ~~comprising~~ including: a timing memory containing predetermined timing data; ~~and~~ a counter for loading timing data output from the timing memory and outputting a pulse signal at a timing indicated by the timing data~~, the timing generation circuit further comprising:~~; and load data switching means for dividing a memory region of the timing memory, selecting one or a plurality of timing data output from the divided memory regions, and loading the selected one or plurality of timing data in the counter to thereby output the pulse signal of one timing indicated by the one or plurality of timing data.

(12) The paragraph from page 6, line 25 to page 7, line 2 has been amended as follows:

Consequently, a timing generation circuit can be easily obtained with low cost which is capable of increasing a maximum delay amount ~~or~~ and also increasing a timing set number without changing a circuit configuration of the timing memory and which is provided with a function optimum for each IC tester (semiconductor test device), ~~and a~~ thereby realizing a timing generation circuit ~~can be realized which is superior in~~ with high versatility and expandability.

(13) The paragraph from page 7, line 4 to page 7, line 10 has been amended as follows:

Moreover, in the timing generation circuit of the present invention, the load data switching means divides the memory region of the timing memory in an address direction by mode switching, links a plurality of timing data output from the divided memory regions in a data bit width direction, and loads these data as one timing data in the counter.

(14) The paragraph from page 7, line 4 to page 7, line 10 has been amended as follows:

Specifically, the load data switching means ~~comprises~~ includes: an address selection circuit which designates one or a plurality of addresses of the timing memory by the mode switching and which outputs one or a plurality of timing data stored in the corresponding one or plurality of addresses; and a load data switching circuit which loads the one timing data as ~~such~~ is in one counter, when one timing data is output from the timing memory by switching, and which loads the plurality of timing data in a plurality of cascaded counters, when a plurality of timing data are output from the timing memory by switching, to thereby output the pulse signal of one timing indicated by the one or plurality of timing data.

(15) The paragraph from page 8, line 1 to page 8, line 8 has been amended as follows:

According to the timing generation circuit of the present invention constituted in this manner, the memory region of the timing memory can be divided in the address direction, and one address can be designated to output a plurality of timing

data. Moreover, when the plurality of timing data are cascaded and loaded in the counter, for example, the pulse signal can be output at the timing indicated by the timing data ~~twice~~ expressed by the bit width two times larger than the standard bit width.

(16) The paragraph from page 8, line 22 to page 9, line 5 has been amended as follows:

Specifically, the load data switching means ~~comprises~~ includes: a data division circuit which divides the timing data stored in one address of the designated timing memory into a plurality of timing data and which outputs the plurality of divided timing data by the mode switching or which outputs one timing data among the plurality of divided timing data; and a load data switching circuit which loads the plurality of timing data in a plurality of cascaded counters, when the plurality of divided timing data are output from the timing memory by the mode switching, and which loads the one timing data as ~~such~~ is in one counter, when one divided timing data is output from the timing memory by switching, to thereby output a pulse signal of one timing indicated by the plurality of or one divided timing data.

(17) The paragraph from page 9, line 22 to page 9, line 26 has been amended as follows:

Consequently, a timing generation circuit can be easily obtained at a low cost, where the timing generation circuit is capable of increasing a timing set number without changing the

circuit configuration of the timing memory ~~and comprising the timing set number~~, thereby establishing any desired number of timing sets optimum for each IC tester.

(18) The paragraph from page 9, line 28 to page 10, line 11 has been amended as follows:

Moreover, according to the present invention, there is provided a semiconductor test device ~~comprising~~ including a timing generation circuit, which inputs a predetermined test pattern signal into a device under test constituting a test object and which compares a response output signal output from this device under test with a predetermined expected pattern signal to thereby judge whether or not the device under test is satisfactory, ~~the semiconductor test device further comprising:~~ and a timing generation circuit which outputs a reference clock signal of the test pattern signal as a delay clock signal delayed by a predetermined time, where the timing generation circuit ~~comprising~~ is configured by any of the above-described timing generation circuits of the present invention.

(19) The paragraph from page 11, line 6 to page 11, line 8 has been amended as follows:

~~FIG. 2 is an explanatory view~~ FIGs. 2(a) and 2(b) are explanatory views schematically showing switching of a timing data length in a timing memory of the timing edge generation unit shown in FIG. 1;

(20) The paragraph from page 11, line 15 to page 11, line 18 has been amended as follows:

~~FIG. 5 is an explanatory view~~ FIGs. 5(a) and 5(b) are explanatory views schematically showing switching of a timing set number in the timing memory of the timing generation circuit according to a second embodiment of the present invention;

(21) The paragraph from page 11, line 27 to page 12, line 1 has been amended as follows:

~~FIG. 8 is an explanatory view~~ FIGs. 8(a) and 8(b) are explanatory views schematically showing a modification of the timing generation circuit according to the second embodiment of the present invention in a case where the memory region of the timing memory is unequally divided in a data bit width direction;

(22) The paragraph from page 12, line 29 to page 13, line 1 has been amended as follows:

~~FIG. 2 is an explanatory view~~ FIGs. 2(a) and 2(b) are explanatory views schematically showing switching of a timing data length in a timing memory of the timing edge generation unit shown in FIG. 1.

(23) The paragraph from page 13, line 5 to page 13, line 8 has been amended as follows:

The first embodiment of the timing generation circuit (timing edge generation unit) of the present ~~embodiment~~

invention shown in these figures is ~~disposed~~ implemented in a semiconductor test device shown in FIG. 10.

(24) The paragraph from page 13, line 9 to line 13 has been amended as follows:

The semiconductor test device inputs a test pattern signal to a semiconductor device under test (DUT) ~~which is a test object~~, compares a response output signal ~~output~~ from the DUT with a predetermined expected pattern signal, and judges agreement/disagreement therebetween to thereby test the DUT.

(25) The paragraph from page 13, line 14 to line 20 has been amended as follows:

Moreover, this semiconductor test device is provided with a timing generation circuit (TG) (see FIG. 10) which generates a timing of a waveform to be applied to the DUT in order to apply a test signal to the DUT at a predetermined timing~~, and as this TG,~~. Instead of the conventional TG, a TG (timing generation circuit) ~~is disposed~~ according to the present embodiment is implemented in the semiconductor test device of the present invention.

(26) The paragraph from page 14, line 18 to page 14, line 24 has been amended as follows:

~~Moreover, when~~ When the counted-down timing data indicates "0", the down counter 20 outputs a pulse signal ("All zero" signal). This pulse signal is input as a timing signal into a pattern generation unit or the like (not shown), and the timing signal is generated which is represented by a

delay time which is an arbitrary integer ~~times~~ multiple of a CLK signal period.

(27) The paragraph from page 14, line 25 to page 15, line 2 has been amended as follows:

Here, the TG of the present embodiment ~~comprises~~ includes a plurality of down counters 20 in the same manner as in the above-described conventional TG, and ~~comprises~~ further includes four-phase down counters 20a to 20d in an example shown in FIG. 1 (see also FIG. 3). Moreover, the four-phase down counters 20a to 20d are provided with a four-input OR gate 23 on an output side~~, and~~ so that the pulse signals are successively taken from the four-phase down counters 20a to 20d.

(28) The paragraph from page 15, line 11 to page 15, line 18 has been amended as follows:

Specifically, as shown in FIG. 3, CO of the first-phase down counter 20a is input into CI of the second-phase down counter 20b by the switching of the mode signal (mode switching), and both the counters 20a, 20b are cascaded, i.e., connected in series. Similarly, CO of the third-phase down counter 20c is input into CI of the fourth-phase down counter 20d by the switching of the mode signal, and both the counters 20c, 20d are cascaded.

(29) The paragraph from page 15, line 23 to page 15, line 30 has been amended as follows:

As shown in FIG. 3, the two cascaded down counters 20a, 20b (or 20c, 20d) are provided with an AND gate 25a (or 25b) on its output side, and the pulse signal of one timing indicated by the two timing data is output. As shown in FIG. 3, the two sets of cascaded down counters 20a, 20b and 20c, 20d are provided with a two-input OR gate 24 on the output side~~, and~~ so that the pulse signals are successively taken from the two sets of down counters 20a, 20b and 20c, 20d.

(30) The paragraph from page 17, line 5 to page 17, line 8 has been amended as follows:

In the present embodiment, when a mode signal "H" ("1") is input, a valid address length is set to 1/2 of the standard address length, and two addresses are simultaneously enabled, ~~and accordingly~~ which means that one address is divided into two addresses.

(31) The paragraph from page 17, line 9 to page 12, line 8 has been amended as follows:

~~To set~~ For setting the valid address length to 1/2 and divide one address into two addresses in this manner, ~~this can be easily realized by disposing~~ a selector which switches MSB of the address to "H" or "L" is provided to easily achieve this purpose.

(32) The paragraph from page 17, line 16 to page 17, line 23 has been amended as follows:

The load data switching circuit 50 loads one timing data as ~~such~~ is in one down counter 20, when one timing data is

output from the TMM 10 by the mode switching, ~~and~~ whereas it loads a plurality of timing data in a plurality of cascaded down counters 20, when a plurality of timing data are output from the TMM 10 by the mode switching, ~~to output~~ thereby outputting the pulse signal of one timing indicated by the one or plurality of timing data.

(33) The paragraph from page 18, line 3 to page 18, line 9 has been amended as follows:

When two timing data are output from the TMM 10, the mode signal "H" ("1") is input into the selectors 50a to 50c to cascade/connect (20a and 20b, 20b and 20d) two of the four down counters 20a to 20d of the next stage. The selectors 50a to 50c load the two timing data in the respective cascaded down counters 20a and 20b, 20c and 20d to output the pulse signal of one timing.

(34) The paragraph from page 18, line 21 to page 18, line 29 has been amended as follows:

Specifically, the timing data selection circuit 60 is constituted of a selector switchable by the same mode signal as that input into the address selection circuit 40~~,~~ and the load data switching circuit 50, and selects/outputs the pulse ~~signal~~ signals successively output from the four-phase down counters 20a to 20d, when the mode signal is "L" ("0"). The timing data selection circuit 60 selects/outputs the pulse ~~signal~~ signals output from the two cascaded down counters 20a, 20b, and 20c, 20d, when the mode signal is "H" ("1").

(35) The paragraph from page 19, line 5 to page 19, line 12 has been amended as follows:

In the present embodiment, in a case where the memory region of the TMM 10 is used as ~~such~~ is, and the timing data having a usual (standard) bit width of ~~a memory~~ the TMM 10 is stored and output (standard delay mode), the mode signal is switched to "L". In a case where the memory region of the TMM 10 is divided, and two or more data are linked to output timing data having a larger delay amount (long delay mode), the mode signal is switched to "H".

(36) The paragraph from page 19, line 18 to page 19, line 24 has been amended as follows:

First, in the standard delay mode in which the memory region of the TMM 10 is used as ~~such~~ is, the mode signal is set to "L". It is to be noted that, in this case, the TG of the present embodiment is usable in the same manner as in the above-described conventional TG (see FIGS. 11, 12).

(37) The paragraph from page 20, line 4 to line 10 has been amended as follows:

Specifically, as shown in FIG. 3, timing data (D<m-1...0> shown in FIG. 3) is set as ~~such~~ is in the first-phase down counter 20a and the third-phase down counter 20c, and the same data (D<m-1...0> shown in FIG. 3) is set in the second-phase down counter 20b and the fourth-phase down counter 20d via the selector 50a of the load data switching circuit 50.

(38) The paragraph from page 20, line 11 to page 20, line 15 has been amended as follows:

The timing data set in the respective down counters 20a to 20d are loaded by the load signal of the counter load enable selection circuit 30, and accordingly ~~make a decrement~~ decremented by one in synchronization with each occurrence of the CLK signal in the respective down counters 20a to 20d.

(39) The paragraph from page 20, line 23 to page 20, line 27 has been amended as follows:

In this standard delay mode, as shown in the table of FIG. 4, the memory region (n×m in the memory shown in FIG. 2) of the TMM 10 is used as ~~such,~~ is, and the timing data is stored and output. Therefore, usable timing data are n sets of data having an m-bit width.

(40) The paragraph from page 21, line 16 to page 21, line 19 has been amended as follows:

Specifically, as shown in FIG. 3, among two m-bit timing data, one m-bit data (D<m-1...0> shown in FIG. 3) is set as ~~such~~ is in the first-phase down counter 20a and the third-phase down counter 20c.

(41) The paragraph from page 22, line 2 to page 22, line 5 has been amended as follows:

Accordingly, the two timing data are linked in the bit width direction of the data, and the bit width of the timing data ~~is~~ becomes twice (2m bits) the bit width (m bits) of the standard delay mode.

(42) The paragraph from page 22, line 6 to page 22, line 13 has been amended as follows:

That is, the timing data set in the respective down counters 20a to 20d are loaded by the load signal of the counter load enable selection circuit 30, and accordingly two timing data are counted down in the two cascaded down counters 20a, 20b (or 20c, 20d). Accordingly, long delay data can be counted which is indicated by the bit width which is ~~twice~~ two times longer than that of the standard delay mode.

(43) The paragraph from page 23, line 1 to page 23, line 10 has been amended as follows:

As described above, in the timing generation circuit of the present embodiment, a plurality of addresses of the memory (TMM 10) are accessed with one address ~~as an access to a memory (TMM 10)~~ for outputting a plurality of bits (m bits) in a total bit number m×n. A switchable flexible configuration can be switched by a minimum control signal (at least one mode signal) which is the mode signal, and the selector circuit without requiring increase/decrease of a memory cell number. ~~A~~ As a consequence, a plurality of memory configurations can be ~~substantially~~ realized by one memory configuration (m×n).

(44) The paragraph from page 23, line 24 to page 24, line 1 has been amended as follows:

Moreover, in the TG of the present embodiment in which different types of TG can be easily mixed using the conventional TG circuit as ~~such~~ is in this manner while

largely suppressing the increase of the circuit scale, the configuration can be realized easily by any IC tester. Therefore, since a function can be optimized/realized at the low cost for each customer, a very useful TG can be provided especially in the IC tester for a ~~row~~ low end.

(45) The paragraph from page 25, line 1 to page 25, line 4 has been amended as follows:

~~FIG. 5 is an explanatory view~~ FIGs. 5(a) and 5(b) are explanatory views schematically showing switching of a timing set number in the timing memory of the timing generation circuit according to the second embodiment of the present invention.

(46) The paragraph from page 25, line 11 to page 25, line 19 has been amended as follows:

A TG of the present embodiment shown in these drawings is a modification of the above described first embodiment. In the TG of the first embodiment, the memory region of the TMM 10 is divided in the address direction to link a plurality of timing data in a data bit width direction (see FIG. 2). On the other hand, in the ~~present~~ second embodiment, the memory region of the TMM 10 is divided in a data bit width direction, and accordingly a TS (timing set) number of usable timing data can be increased.

(47) The paragraph from page 25, line 28 to page 26, line 5 has been amended as follows:

As shown in ~~FIG. 5~~ FIGs. 5(a) and 5(b), in the present embodiment, load data switching means divides the memory region of the TMM 10 in the data bit width direction by switching of a mode signal (mode switching), and selects one timing data from the timing data output from the divided memory regions to load the timing data in the down counter 20. Accordingly, the timing set number (TS number) of usable timing data can be increased without changing the memory configuration of the TMM 10.

(48) The paragraph from page 26, line 6 to page 26, line 9 has been amended as follows:

Specifically, the load data switching means of the present embodiment ~~comprises~~ includes a data division circuit 70 shown in FIG. 6, a load data switching circuit 50 shown in FIG. 7, and a timing data selection circuit 60 ~~(not shown)~~ equivalent to that shown in FIGs 1 and 3.

(48) The paragraph from page 26, line 17 to page 26, line 21 has been amended as follows:

The data division circuit 70 divides the timing data stored in one designated address of the TMM 10 into a plurality of timing data, and outputs a plurality of divided timing data by the switching of the mode signal, or outputs one timing data among the plurality of divided timing data.

(49) The paragraph from page 27, line 18 to page 27, line 21 has been amended as follows:

The MSB-side selector 70a ~~enables write into~~ write-enables the MSB-side memory 10a of the corresponding address by the switching of the mode signal, when MSB of one address value of the designated TMM 10 indicates "H" ("1").

(50) The paragraph from page 27, line 22 to page 27, line 24 has been amended as follows:

The LSB-side selector 70b ~~enables write into~~ write-enables the LSB-side memory 10b, when MSB of the address value indicates "L" ("0").

(51) The paragraph from page 28, line 4 to page 28, line 8 has been amended as follows:

First, two selectors 70a, 70b ~~enables~~ enable the valid addresses of both the memories 10a, 10b regardless of a value (Adr<x-1> shown in FIG. 6) of MSB of a designated address (Adr<x-1...0> shown in FIG. 6), when the mode signal indicates "L" ("0").

(52) The paragraph from page 28, line 22 to page 28, line 26 has been amended as follows:

On the other hand, when the mode signal indicates "H" ("1"), two selectors 70a, 70b ~~switches a~~ switch the valid address to be enabled in accordance with the value (Adr<x-1> shown in FIG. 6) of the MSB of the designated address (Adr<x-1...0> shown in FIG. 6).

(53) The paragraph from page 29, line 16 to page 29, line 23 has been amended as follows:

The load data switching circuit 50 loads a plurality of timing data in a plurality of cascaded down counters 20, when a plurality of divided timing data are output from the TMM 10 by switching, and loads one timing data as ~~such~~ is in one down counter 20, when one divided timing data is output from the TMM 10 by the mode switching, to output the pulse signal of one timing indicated by the divided plurality of timing data or one timing data.

(54) The paragraph from page 30, line 9 to page 30, line 18 has been amended as follows:

Specifically, when MODE does not rise, that is, the mode signal indicates "L" ("0"), the valid bit of the timing data of the TMM 10 has a usual bit width (m bits). Therefore, the load data switching circuit 50 sets the MSB-side timing data (DOUT MSB shown in FIG. 7) in the down counters 20a to 20n. At this time, the LSB-side timing data (DOUT LSB shown in FIG. 7) is set as ~~such~~ is in the down counters 20a to 20n. Accordingly, the timing indicated by the m-bit timing data is counted down in the down counters 20a to 20n.

(55) The paragraph from page 31, line 9 to page 31, line 19 has been amended as follows:

In this case, the counters are assembled beforehand in such a manner that the m/2-bit down counters 20a to ~~0n~~ 20n are constituted as shown in FIG. 3 in such a manner as to obtain a valid data bit number of m/2 at a time when the mode signal is indicated "H" ("1"). Accordingly, in MODE = 0, i.e., the

mode signal is indicated "L" ("0"), the selectors are assembled (see the selectors 50a to 50c of FIG. 3) in such a manner ~~as to obtain~~ to establish cascade connection of two of m/2-bit down counters 20a to 20n (in the same manner as in FIG. 3), N-phase m-bit counters are constituted, and 2N-phase m/2-bit down counters can be operated in MODE = 1.

(56) The paragraph from page 32, line 23 to page 32, line 25 has been amended as follows:

As shown in ~~FIG. 8~~ FIGs. 8(a) and 8(b), when the memory region of the TMM 10 is divided in the data bit width direction, the bit number may be unequally divided.

(57) The paragraph from page 33, line 26 to page 33, line 26 has been amended as follows:

~~Industrial Applicability~~